Sample of Level 2 Editing with Target Tutoring

A 0.2-to-34 GHz Novel Ring-Based Triple-Push ~~V~~VCO in 0.13µm CMOS Technology

A novel ring-based triple-push voltage-controlled oscillator (VCO) with a continuous range from 0.2 to 34 GHz is proposed and realized using the~~in~~ commercial 0.13-µm 1P8M CMOS VCO process. The output power of the VCO is -18 dBm and there is~~with~~ a ± 2 dB variation in the full band. The fundamental rejection is more than~~above~~ 15 dB and the second harmonic rejection is more~~better~~ than 25 dB. This VCO achieves the widest continuous~~ly~~ tuning range reported to date~~a~~.

The local oscillator is a key component in ~~wide band~~wideband and ~~high speed~~high-speed applications. T~~Due to t~~he ~~ever increasing~~ever-increasing demand for bandwidth makes~~,~~ the tuning range of the voltage-controlled oscillator (VCO)~~ is~~ an important factor~~eature~~ in the production of microwave and millimeter-wave frequencies~~y~~. ~~Due to the fixed inductors,~~ M~~m~~ost LC VCOs are ~~usually~~ used for narrow band design due to fixed inductors [1],[2],[4]. S~~There are s~~everal ~~approaches to enhance~~approaches can be used to enhance the tuning range~~,~~, which include~~-~~ the use of a~~such as~~ switch capacitor, an~~or~~ inductor, a duplicate oscillator or~~and~~ frequency mixing [3]. Most of these approaches~~them~~ consume large chip size and complex design in system. Ring oscillators can easily achieve a wide tuning range with a small chip size, but they suffer from ~~the~~ oscillation frequency limitations and high power dissipation at high frequency. For example, the highest fundamental ring oscillator in a SiGe HBT with f_T of 120 GHz is proposed at 32 GHz in [5].

~~In stead of adopting high f_{max} process technology,~~ There are c~~there are e~~ircuit

Comment [a1]:
TUTOR - convention:

You have included the expansion of 'VCO' later inthe document. It would be better to include it the first time the term is used.

Comment [a2]: CHECK: It would be better to clarify to the reader what you mean by 'realized' here. Also, what exactly is the 0.13-µm 1P8M CMOS VCO, if it is an example of this kind of VCO, you may want to make that clear to the reader.

Comment [a3]:
TUTOR - Word choice:

OK: 'better'
Better: 'more'
Reason: With a numeric quantity, it is better to use terms like 'more' rather than using terms like 'better' which do not convey as much information to the reader.

Comment [a4]: CHECK: Did you mean to say 'reported to date' here?

Comment [a5]: CHECK: What is an LC VCO? Please mention that here.

Comment [a6]: CHECK: The meaning of this sentence is unclear, please rephrase.

Comment [a7]: CHECK: The meaning of 'is proposed' in this sentence is unclear, please rephrase. Perhaps you meant to say 'is limited to 32 GHz'?

Comment [a8]: CHECK: Is this a known technical term? IF not, you may want to change it to make the meaning clearer.

structures that could be used instead of adopting high f_{max} process technology, to~~to~~ increase the tuning range ~~as well as to~~and to achieve higher oscillation frequencies. The multi-push VCO is an attractive choice because it cancels the fundamental signals and sums up the desired in-phase multiple harmonics as the output signal. In traditional topologies~~y~~, it is usually composed of several identical oscillators. However, the multi-push VCO~~, but it~~ has the problems~~disadvantage~~ of large chip size and process variation [6].

A new topology is proposed t~~T~~o overcome the frequency limitation of a ring oscillator~~, a new topology is proposed~~. Fig.~~ure~~ 1 shows the block diagram of a multi(M)-push topology with an N-stage ring oscillator.~~,~~ H~~wh~~ere, M could be ~~the~~ a factor of N. The oscillation frequency of a ring oscillator can be derived using~~by~~ the multi-push M, the current Ictrl, the number of stages N, the amplitude V_{osc} and the parasitic capacitance CG. In Fig.1, large number of stage brings up low frequency. To decrease the effect in frequency from number of stage, the value of M can be set~~lected~~ equal~~s~~ to N. This enhances~~Then,~~ the oscillation frequencies~~y~~ of different stages ~~is enhanced~~ and brings them closer to each other~~close to each other~~. ~~Due to the large power consumption and complex layout routing~~ , The use of more~~more number of~~ stages is not recommended since it would result in large power consumption and complex layout routing ~~suggested~~. ~~Furthermore, the value~~The highest frequency is seen when the values of both M and N are equal to three (Fig. 1). ~~of M and N equals to three shows the highest frequency in the comparison, as shown in Fig. 1.~~ In this paper, the use of a ~~VCO which combines the three-stage ring oscillator and triple-push topology~~VCO that combines the three-stage ring oscillator and the triple-push topology is proposed in a commercial 0.13- m 1P8M CMOS process. The triple-push approach enhances the oscillation frequency and the tuning range of a ring oscillator. It also ~~greatly~~ reduces~~saves~~ the power dissipated~~ion~~ in a ring oscillator at high frequency. An appropriate

Comment [a9]: CHECK: Is this a known technical term? IF not, you may want to change it to make the meaning clearer.

Comment [a10]: TUTOR: This sentence is well written and well structured.

Comment [a11]: CHECK:
Is the term commonly written as 'multi-push' or 'multi push'? Please use the term the same way throughout the document.

Comment [a12]: CHECK: You may want to clarify what is meant by 'process variation' here.

Comment [a13]:
TUTOR – Grammar:
Incorrect: a N-stage
Correct: an N-stage
Reason: When pronouncing 'N' the sound starts with a vowel (read: en). Therefore, use 'an'.
Example: A T-stage…
Example: An N-stage…
Example: An M-stage…

Comment [a14]: CHECK: The meaning of this sentence is unclear, please rephrase.

Comment [a15]: CHECK: The meaning of this sentence is unclear, please rephrase.

Comment [a16]: CHECK: Is enhances the word you would like to use here? Perhaps 'increases' would be more appropriate?

Comment [a17]: CHECK: Is this the correct interpretation of the meaning of this sentence?

Comment [a18]: TUTOR - Word choice:
OK: 'saves power'
Better: 'reduces the power dissipated'
Reason: It is better to say that the power is 'reduced' rather than 'saved' in this context since only the power usage in the experiment is relevant to the reader.

Comment [a19]: TUTOR -Word Choice:
The use of words like 'greatly' should be avoided when no specific value is given. e.g. Here 'greatly' conveyed no meaning since it did not convey any additional informa… [1]

topology for the triple push approach is a~~In addition, a~~ three-stage ring oscillator since it~~that~~ can ~~naturally~~ provide three signals with a 120^{o} phase shift ~~is an appropriate topology for the triple push approach~~. Since there is only the odd ~~-~~mode in three-stage ring oscillator, the fundamental and second harmonics will cancel out. In the~~The~~ circuit schematic ~~is~~ shown in Fig. 2,~~-~~ a~~A~~ conventional ring oscillator with a PMOS as resistive load and current control and ~~is used as well as~~ a 16-finger NMOS with a total gate width of 32 µm are used.~~,~~ The circuit also uses~~and~~ a 12-finger PMOS with a total gate width of 120 µm which~~to~~ ensures that the ~~a small~~ voltage drop between the drain and the source is small. The NMOS device trade off between the parasitic capacitance and the transconductance to reach the highest frequency. The PMOS device is chosen to have a~~selected to~~ large gate width to lower the ~~voltage~~ drop in V_{DS}.~~;~~ However, the large gate width~~but~~ causes~~it results in~~ a decrease~~sing~~ in the~~of~~ oscillation frequency.

In the tuning mechanism, the gate bias of the PMOS is selected so that it~~controlled to~~ turns on the current through the NMOS. The breakdown voltage between the gate and the source in the PMOS determines t~~T~~he lower~~st~~ limit of the control voltage ~~is limited by the breakdown voltage between the gate and the source in the PMOS.~~; ~~where~~ Here, the PMOS provide the highest current, and~~and the PMOS~~ is in the~~to~~ triode region. The PMOS offers a~~provides~~ low resistance, which ~~to~~ reduces the RC delay. The upper~~highest~~ limit of the control voltage is the current level that satisfies the oscillation condition. In this case,~~where~~ the PMOS is in the saturation region and offers a~~provides~~ high resistance to low frequency oscillations~~e in low frequency~~. ~~In order to make the oscillation frequency as high as possible,~~ All the~~every~~ parasitic capacitances in the loop should be reduced to make the oscillation frequency as high as possible.~~-~~ The current source is removed to decrease the noise source and enhance the voltage ~~head room~~headroom. Since~~Because~~ a~~the~~ larger~~higher~~ current generates

Comment [a20]: CHECK: Do you mean to say ‘an odd mode’ or ‘odd modes’? The meaning of the word ‘only’ is unclear, perhaps you meant to say ‘there is an odd mode and no even modes’?

Comment [a21]: CHECK: The meaning here is unclear. Do you mean to say 'The NMOS device is a trade off' or 'The NMOS trades off'? Please rephrase the rest of the sentence accordingly.

Comment [a22]: CHECK: IS this what is meant by this sentence?

Comment [a23]: CHECK: The meaning here is unclear. When you say 'highest current', what are you comparing the current to? And do you mean to say 'when' instead of 'where'?

Comment [a24]: CHECK: Did you mean to say that the 'PMOS' offers low resistance or did you want to refer to something else?

Comment [a25]: TUTOR - Sentence structure:

This sentence conveyed a lot of information that made it difficult to read. To improve readability, it is better to express it in multiple sentences.

Comment [a26]: CHECK: The meaning here is unclear. You are comparing a voltage to a current.

Comment [a27]: CHECK: The meaning here is unclear, please rephrase.

Comment [a28]: TUTOR- Sentence Structure:
In order to improve readability, it better to state the conclusion at the end of this sentence, after giving the relevant information.

Comment [a29]: CHECK: Did you mean to say ‘source noise’ here?

larger~~higher~~ output power at a high frequency, the output power increases with the frequency. As the power gain degrades at high frequency, t~~T~~he common source buffer is used to flatten the curve of the output power versus the tuning frequency. ~~due to the degradation of power gain at high frequency~~ This~~and thus~~ prevents the loading effect from~~from~~ the transmission lines due to power combination~~ing~~. The size of the buffer, a 12-finger NMOS with 24-µm gate width, is a trade off between the parasitic capacitance and the flatness of output power.

~~In order to enhance the fundamental and the second harmonic rejection, A~~any asymmetry in the loop in terms of phase errors or process variation should be minimized to enhance the fundamental and the second harmonic rejection. A t~~T~~hin-film microstrip (TFMS) line ~~(TFMS)~~ is used to combine the three signals after the drain of buffers. Each drain of the PMOS is connected to the V_{DD} with an equal length~~s~~ of TFMS. The gates are biased using~~through~~ 5 *k*Ω resistors. The control voltage and V_{DD} are ~~naturally~~ virtually short by nature.

Measurements on t~~—T~~his CMOS VCO ~~is measured~~are carried out by ~~via~~ on-wafer probing. Measurements on the~~The~~ output port are done~~is measured~~ through bias-T. Fig. 3 shows the measured current and control voltage versus the oscillation frequency. The output frequency can be ~~continuously~~ tuned continuously in the range~~from~~ 0.2 GHz to 34 GHz. ~~with~~ T~~t~~he control voltage varies~~ying~~ between~~from~~ 1.75 V and~~to~~ 0.85 V, and~~with~~ the core current var~~y~~ies~~ng~~ from 0.5 mA to 35 mA. The V_{DD} is 2 V, and the buffer is 0.7 V with 7 mA. The output power is -18 dBm with a ±2dB variation, as is shown in Fig. 4. The measured fundamental rejection is more than~~above~~ 15 dB and the second harmonic rejection is more than 25 dB. The phase noise for a~~at~~ 1 -MHz offset frequency ranges from -75.6 dBc/Hz to -69.2 dBc/Hz and for a~~at~~ 10-MHz offset frequency, it ranges from -98.3 to -92.6 dBc/Hz. The phase noise has a degrades by~~ation~~ of 9.54 dBc compared to~~from~~ the fundamental phase noise

Comment [a30]: CHECK: IS this what you meant to say with this sentence? In particular, please check if 'degrades' is the correct term to use.

Comment [a31]: CHECK: Did you mean to say 'draining of the buffers' or are there specific drains you refer to?

Comment [O32]: TUTOR- Conventions:
OK: 5kΩ
Better: 5 kΩ
Reason: It is better to have a space between the number and the unit, and to use the same convention throughout the document. You have used no space, or a hyphen in some places.

Comment [a33]: TUTOR – Phrasing: It should be clear what a verb is being associated with, for example in this sentence, it was not clear what was being measured.

Comment [a34]: CHECK: Is '0.2' GHz the correct value here? If so, you may want to use '200 MHz' instead.

Comment [a35]: CHECK: Does the voltage 'vary between 1.75V and 0.85V' or 'change from 1.75V to 0.85V'?

Comment [a36]: CHECK: Please rephrase, the meaning is unclear.

Comment [a37]: CHECK: The meaning of this part of the sentence is unclear, please rephrase.

due to the triple-push mechanism. Fig. 5 shows~~depicts~~ the chip photo of the triple-push VCO~~.~~, It has~~showing~~ a compact chip size of 0.34 x 0.28 mm^2, which ~~-~~includes~~ing~~ the area of the pads. The core area is only 0.19 x 0.13 mm^2. Fig. 6 lists the performance of recent~~recently~~ wide-band Si-based VCOs. The~~This~~ work that this paper talks about achieves the widest tuning range and smallest chip size.

A ring-based triple-push VCO that~~which~~ is continuously tuneable from 0.2 to 34 GHz ~~has been proposed~~was proposed. Using the triple-push topology, t~~T~~he tuning range is tripled~~tripled in the triple-push topology~~ with ~~a~~ good linearity. Due to the absence of inductors, the~~a very small~~ chip size, including the bonding pad is very small~~, is achieved~~. To the best of the author~~'~~s' knowledge, this VCO offers ~~achieves~~ the widest continuous tuning range and the smallest chip size among all of the VCOs reported to date. It demonstrates the potential for ~~wide band~~wideband applications in the~~from~~ microwave to millimeter wave regime in CMOS technology.

Comment [a38]:
TUTOR - Word choice:
When comparing two quantities, it is better to use the word 'compare' rather than saying 'from'.

Comment [a39]:
TUTOR - Phrasing:
When you use terms like 'widest', 'smallest' you need to mention what you are comparing to

Example: …the design achieves the widest tuning range among a certain class of VCOs.

Comment [a40]: CHECK: Please explain what 'good' linearity means.

Comment [a41]:
TUTOR – Grammar:
Since there are multiple authors the apostrophe (') appears after the 's'.

Comment [a42]: CHECK: Did you mean to say 'range' here?

References:

[1] G. Cusmai, M.Repossi, G. Albasini, F. Svelto, " A 3.2-7.3 GHz Quadrature oscillator with Magnetic Tuning" *ISSCC Dig. Tech. papers*, pp. 92-93, Feb., 2007.

[2] K. Kwok, John R. Long, Joh J. Pekarik, "A 23-to-29 GHz Differential Tuned Varactorless VCO in 0.13µm CMOS" *ISSCC Dig. Tech. papers*, pp. 194-195, Feb., 2007.

[3] A. Ismail1, A. Abidi, "A 3.1 to 8.2 GHz Direct Conversionn Receiver for MB-OFDM UWB Communications" *ISSCC Dig. Tech. papers*, pp. 208-209, Feb., 2005.

[4] B. Jung, R. Harjani, "A 20GHz VCO with 5GHz tuning range in 0.25µm SiGe BiCMOS", *ISSCC Dig. Tech. papers*, pp. 178-179, Feb., 2004.

[5] Wei-Min Lance Kuo, J.D. Cressler, Yi-Jan Emery Chen, and A. J. Joseph," An inductorless Ka-band SiGe HBT ring oscillator," *IEEE Microwave and Wireless Comp. Letters*, vol. 15, pp. 682-684, Oct. 2005.

[6] Yu-Lung Tang and Huei Wang, "Triple-push oscillator approach: theory and experiments," *IEEE Journal of Solid-State Circuits*, Vol. 36, pp. 1472-1479, Oct. 2001.

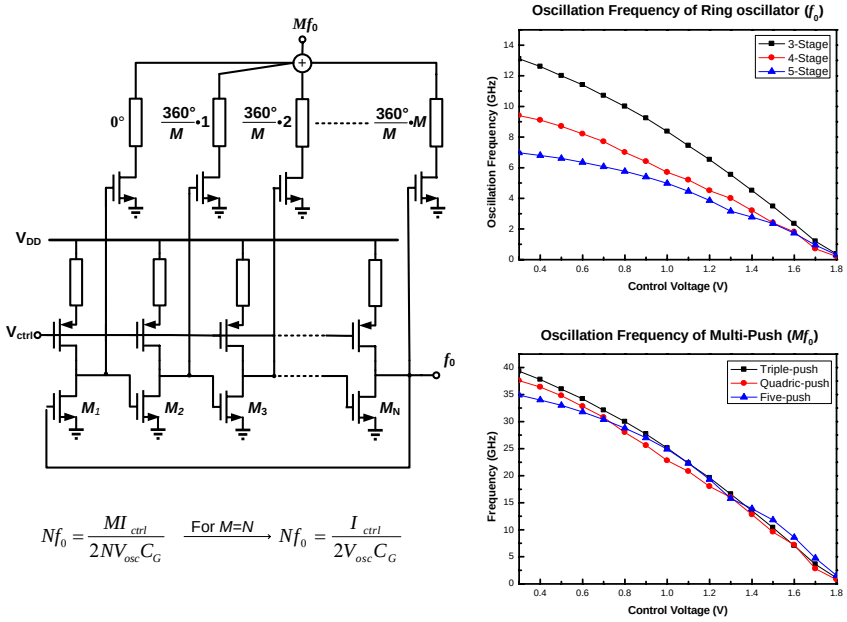

Figure 1: Ring-based multi-push topology and simulated oscillation frequency comparison of multi-stage.

Comment [a43]: CHECK: It may be better to separate these images and use different captions to avoid confusing the reader. You could label the images using a, b, c etc.

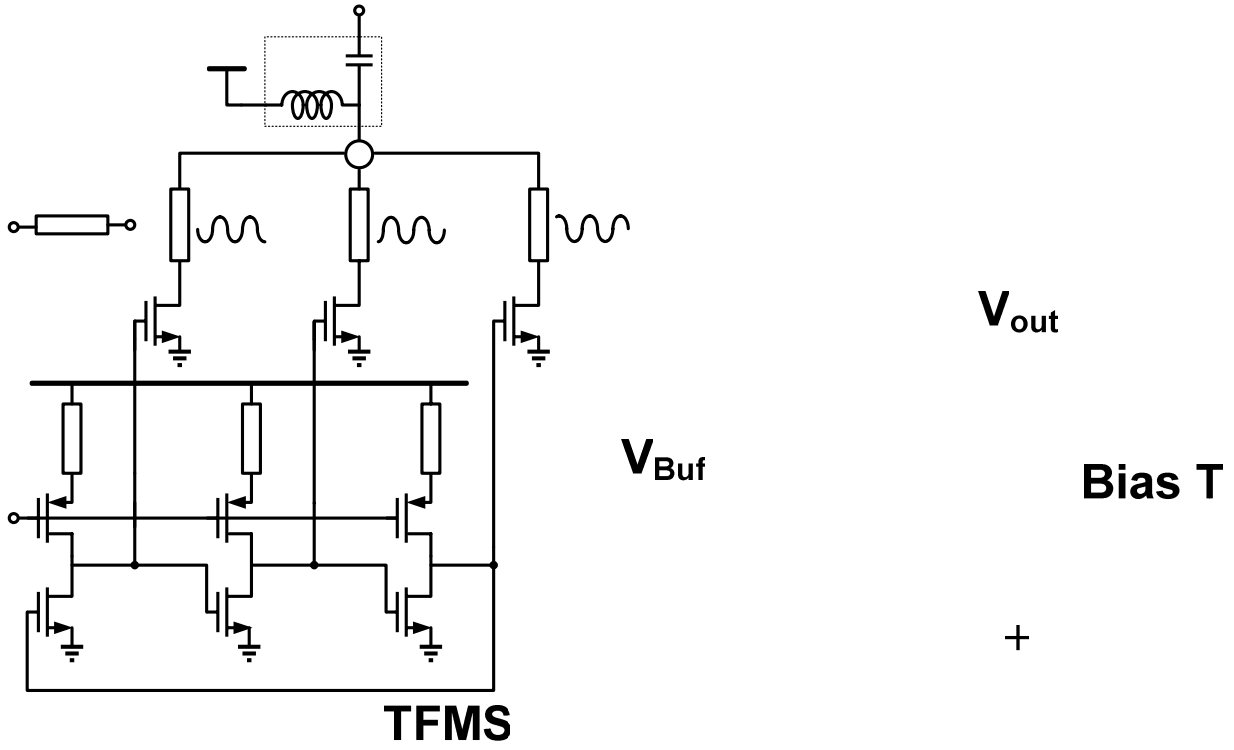

Figure 2: ~~STThe s~~chematic of the ring-based triple-push VCO.

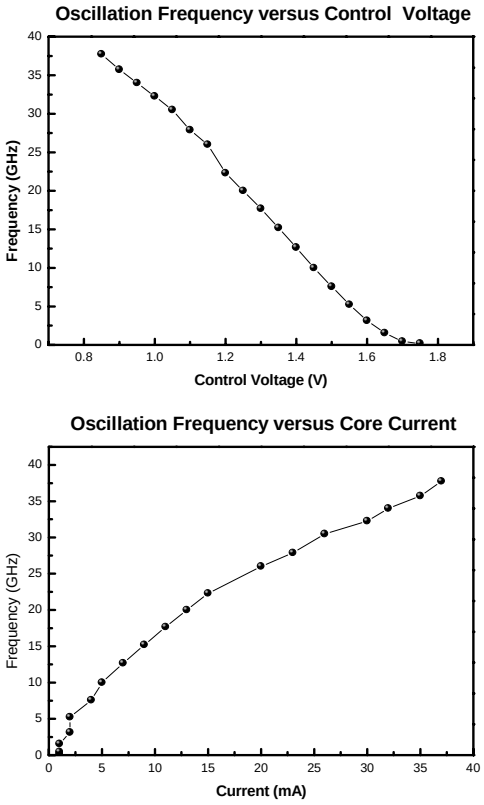

Figure 3: Tuning Characteristics.

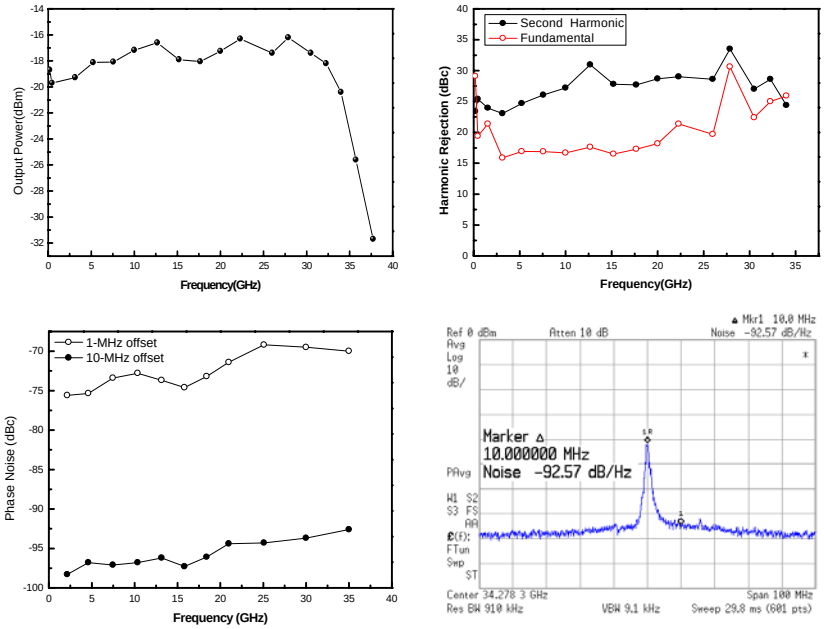

Figure 4: Measurement results.

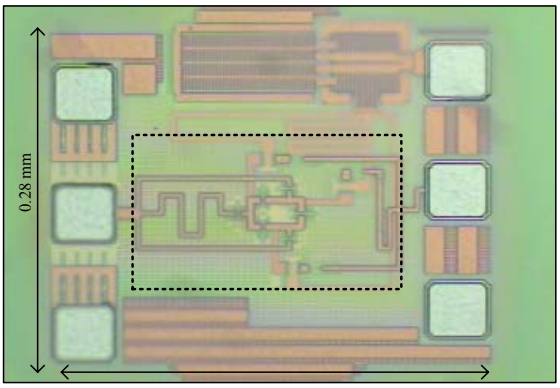

Figure 5: Chip photo of the triple-push VCO with a chip size of 0.34 x 0.28 mm^2

V_{DD}

Core

V_{ctrl}

$3f_0$

0.34 mm

Oscillation Frequency /Process	Phase noise (dBc/Hz)	Core DC power (mW)	Tuning range (GHz) and Percentage(%)	Frequency Ratio (F_{max}/F_{min})	Chip Area (mm^2)	Reference
34 GHz 0.13-µm CMOS	-98.3 @ 10-MHz	2-70	0.2-34 (197.6 %)	170	0.095	This Work
7 GHz 65-nm CMOS	-110 dBc @ 1-MHz	7.2- 42	3.2-7.3 (78 %)	2.3	0.2 (Active area)	[1]
29.4 GHz 0.13-µm CMOS	-96.2 dBc @ 3-MHz	36.5	23.2-29.4 (23.6%)	1.26	1.4	[2]
23 GHz 0.25-µm SiGe BiCMOS	-101.2 dBc @ 1-MHz	9	18-23 (24.3 %)	1.28	--	[4]
32GHz f_T/120 GHz SiGe HBT	-85.3dBc @ 1-MHz	87	28-32 (13.3%)	1.14	0.28	[5]

Figure 6: Summary of measured performance and comparison with recently reported ~~wide band~~wideband VCOs~~.~~

Page 2: [1] Comment [a19] abeer 2008/2/7 11:07:00 PM

TUTOR -Word Choice:

The use of words like 'greatly' should be avoided when no specific value is given. e.g. Here 'greatly' conveyed no meaning since it did not convey any additional information to the reader.